Electronic Version
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# Claims

[c1] 1.A process for stacking chips comprising:
forming insertion pins connected to an insertion-pin frame by necks, the insertion pins having a pitch matching a pitch of pins on a first chip;
wherein the insertion pins and the insertion-pin frame are flat and co-planar;
applying a first solder paste to a first surface of the insertion pins;
aligning the first chip to the insertion-pin frame and placing first pins of the first chip onto the first solder paste on the first surface of the insertion pins;
re-flowing the first solder paste by heating the insertion pins and the first pins to generate a first intermediate assembly;
applying a second solder paste to a second surface of the insertion pins, the second surface opposite the first surface;
aligning a second chip to the insertion-pin frame and placing second pins of the second chip onto the second solder paste on the second surface of the insertion pins;
re-flowing the second solder paste by heating the insertion pins and the second pins to generate a second in-

termediate assembly; and

detaching the insertion pins from the insertion-pin frame by breaking the necks between the insertion pins and the insertion-pin frame to form a final assembly of the first chip, the second chip, and the insertion pins, whereby the first chip is stacked with the second chip using the insertion pins that are flat and co-planar.

[c2] 2.The process for stacking chips of claim 1 further comprising:

inverting the first chip before aligning the first chip to the insertion-pin frame and placing first pins of the first chip onto the first solder paste on the first surface of the insertion pins; and

inverting the first intermediate assembly before applying the second solder paste.

[c3] 3.The process for stacking chips of claim 2 further comprising:

forming a jumper connection from a first pin location to a second pin location on the second chip.

[c4] 4.The process for stacking chips of claim 3 wherein the first pin location is a no-connect pin and the second pin location is a chip-select pin input.

[c5] 5.The process for stacking chips of claim 3 further com-

prising:

forming the jumper connection as a bridge pin between two adjacent insertion pins, the bridge pin having a cutout to prevent soldering of a first pin that is the chip-select pin input to a first surface of the bridge pin;

wherein second pins for the chip-select pin input and the no-connect pin of the second chip are soldered to a second surface of the bridge pin.

[c6] 6.The process for stacking chips of claim 3 further comprising:

placing an insulated wire with stripped ends between the second surface of the insertion pins and the second pins before re-flowing the second solder paste;

wherein the insulated wire is a jumper connection from a first pin location to a second pin location on the second chip.

[c7] 7.The process for stacking chips of claim 3 further comprising:

forming the jumper connection as a bridge between two non-adjacent insertion pins, the bridge being connected to the insertion-pin frame by bridge necks; and

detaching the bridge from the insertion-pin frame by breaking the bridge necks.

[c8] 8.The process for stacking chips of claim 7 wherein the

bridge surrounds a first plurality of the insertion pins; wherein the bridge is connected to the first plurality of the insertion pins by holding tabs;
wherein the holding tabs are removed by punch equipment.

[c9] 9.The process for stacking chips of claim 7 wherein detaching the bridge from the insertion-pin frame comprises using punch equipment to remove the bridge necks.

[c10] 10.The process for stacking chips of claim 7 wherein the bridge is outside of a gap under the second chip and above the first chip.

[c11] 11.The process for stacking chips of claim 4 wherein the first chip and the second chip are memory chips.

[c12] 12.The process for stacking chips of claim 11 wherein the first chip and the second chip are dynamic-random-access memory (DRAM) chips or flash-memory chips.

[c13] 13.The product made by the process of claim 1, wherein the product is the final assembly of the first chip, the second chip, and the insertion pins.

[c14] 14.The process for stacking chips of claim 1 further

comprising:

using a middle insertion-pin frame with middle insertion pins to bond an upper final assembly to a lower final assembly to produce a 4-chip stack,

wherein the upper final assembly and the lower final assembly are each a final assembly produced by the process of claim 1.

[c15] 15.The process for stacking chips of claim 1 wherein re-flowing the second solder paste by heating comprises heating to a lower temperature than a temperature for re-flowing the first solder paste by heating.

[c16] 16.A method of manufacturing a stacked-chip assembly comprising:

printing regions of first solder paste onto first co-planer surfaces of insertion pins that are connected to an insertion-pin frame by frame necks;

placing top shoulders of lower pins of a lower chip into the regions of the first solder paste and heating the first solder paste to produce a first intermediate assembly;

printing regions of second solder paste onto second co-planer surfaces of insertion pins;

wherein the first co-planar surfaces are opposite the second co-planar surfaces;

placing feet of upper pins of an upper chip into the regions of the second solder paste and heating the second

solder paste to produce a second intermediate assembly; and

breaking the necks to detach the insertion-pin frame from the second intermediate assembly with the insertion pins to generate the stacked-chip assembly,

whereby the stacked-chip assembly of the upper chip and the lower chip is held together by the insertion pins that have co-planar surfaces.

[c17] 17.The method of claim 16 wherein non-adjacent upper pins are bridged using a wire under the upper pins, or an outer bridge outside of the frame opening,

wherein the outer bridge is formed from the insertion-pin frame.

[c18] 18.The method of claim 16 wherein adjacent upper pins are bridged using a bridge pin that is soldered to the feet of two upper pins and soldered to the top shoulder of only one of two lower pins.